ASSEMBLY CONCERNS FOR TEST IN STRIP

Bob Fenton
Electroglas, Inc.
San Jose, CA, USA

ABSTRACT
Over the last few years, many of the world's leading semiconductor manufacturers and assembly and test subcontractors have begun testing packaged devices in lead frame, strip or panel format prior to device or package singulation. Test technology advances such as BIST, DFT and higher parallel testers for all applications will accelerate this trend to matrix or strip testing. As more manufacturers adopt strip testing, greater throughput and flexibility will be required to deal with the dual challenges of increasing cost pressure for metal lead frame devices and the difficulties of contacting the geometries of the latest generation of chip scale packaging. Additionally, new assembly parameters must be considered as they relate to suitability to implement strip testing.

This paper examines the implications of assembly methodology on strip testing. First a short overview of why strip testing is becoming more prevalent followed by case studies of actual strip test implementations. Assembly characteristics such as strip or substrate construction, density and geometry are discussed, emphasizing their effects on overall final test efficiency for several different device types, packages and assembly parameters.

Key Words: Final Test, Leadframe, Strip, Matrix, Handler, Wafer Prober.

The concept of conducting final test of packaged semiconductor chips while they are still in assembly matrix format has been around for many years, with many early pre-production lines beginning in the mid to late 1990's. In fact, almost all major integrated device manufacturers and assembly and test contractors have some strip testing programs and capabilities today.

ECONOMICS – TEST CELL THROUGHPUT, COSTS AND CASE STUDIES

What is the cost of test benefit of strip test? This is not an easy to answer question, as the costs vary based on the device type, packaging and application. One of the best ways to illustrate the potential is through the use of case studies. Cost of test is lower in strip test than conventional singulated handling because the throughput of a strip test cell is often many times higher than an equivalent singulated test cell. Here's a formula for estimating strip test handler throughput:

$$I_t=BP_{it}+S_{it}*N$$

Where
I_t = Total strip index time
BP_{it} = strip to strip index time (should include alignment time and soaking)
S_{it} = Stepping time within a panel (should include Z overtravel)
N = Number of test insertions in a strip

$$UPH=3600/(BP_{it}+N(S_{it}+T)) * n$$

Where
UPH = Throughput in units per hour
n = Number of devices in a strip
T = Test time for one insertion

Number of test insertions is normally the number of devices in a strip divided by the tester parallelism, but you will need to factor geometry of the strip and contactor to determine best case stepping within a given strip. This is a typical prober issue with array (multi-site) probing, but is much easier in strip testing because both the strip and the contactor are square or rectangular.

The results of this formula give the following economic benefits.

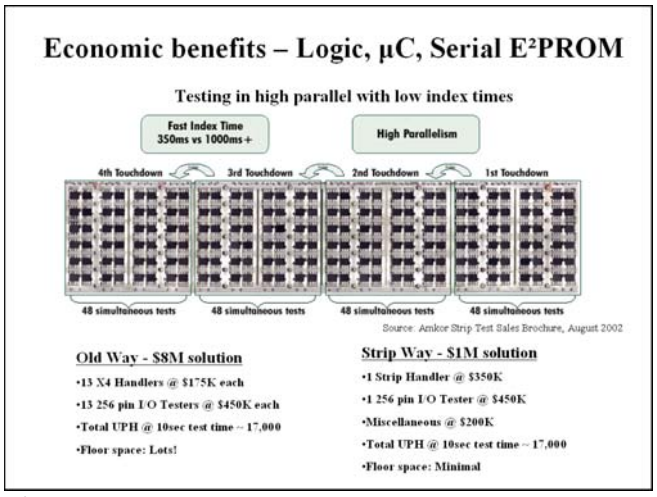

Figure 1

Another example is an application running 28 ball µBGA packages, with 15 to 30 seconds of test time. These might be consistent with FLASH, SRAM or other memory applications. The µBGA 28 packages are in a fairly high-density strip of 192 devices per panel. The traditional

singulated test/mark/pack facility would require the following equipment:

224 units of package dependent capacity
- 12 8-site testers @ $600K each
- 12 8-site handlers @ $350K each
- 4 32-site testers @ $1350K each
- 4 32-site handlers @ $500K each
- 5 Singulated inspection/taping systems @$400K each

Total: About $18 Million in equipment
- Production capability probably less than 24,000 UPH
- Does not include change kits for handlers

About $0 invested in software
- Software "not required" – paper trail, bin boxes, red trays.
- "Never" have any process problems, test escapes, etc.

Add equipment in linear relationship to capacity

By contrast, the equivalent costs/output for a strip-based end of line (EOL) solution would look like this:

250 Units of package independent capacity
- 1 Multi-site, multifunction tester @ $2M
- 1 Sidewinder @ $400K each
- 1 Laser Marker @ $200K
- 4 Singulation/sort saws @ $675K each (also used for isolation pre cuts)
- Strip mapping and process software - $800K

Total: About $5.4M in equipment, $1M in software

Incremental cost of expansion less, more leverage as volume increases
- Next 5K UPH ramp less than $1M!
- Tester PEMs (32 test sites) $250K
- Probe cards/contacts - $50K
- Singulation/Sort cell - $675K

Still $20M per 24K UPH for the old way

At 87K UPH: $28M using strip test; $60M the old way

A final case study is a linear or discrete application. This application features a small Surface Mount Technology (SMT) package – that is approximately 1mm X 0.5mm. In strip format there are many thousands of units in a single array. This application also features a very short test time – 100mS or less.

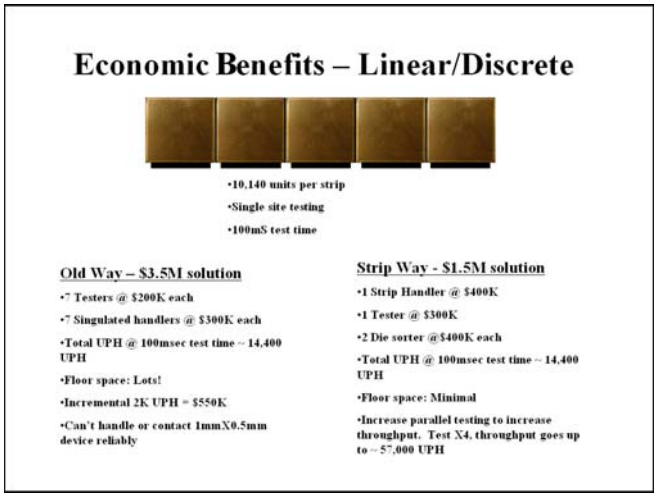

Figure 2

There are several other reasons driving the adoption of strip testing, such as a need to address the inadequacies of mechanically handling small singulated devices and the potentially higher test yields due to more accurate contacting.

Of course, every silver lining has a cloud, and while final test economics dramatically favor strip testing for many package types, there are several hurdles in the way of successful implementation. Those include organizational resistance to process change, existing test capability, overall economics, and – of course assembly methodology.

A BRIEF HISTORY – TRADITIONAL TEST HANDLERS

To truly understand the potential benefits of strip handling and new assembly requirements, one must first understand the history of package test handling and how it has evolved. In the past, test handlers were developed without a lot of concern for or interaction with package assembly.

The first test handlers were gravity fed machines designed to handle Dual Inline Packages. Systems like the Symtek 300 and MCT 3608 were among the main competitors in this arena. As packages evolved, so did gravity handlers, but to start, all handlers seemed to be more or less modified versions of these core machines.

The base concept was to have the packages slide down an inclined rail up to a retractable stop where they are touched by electrical clamps for testing. Below the test site there was a shuttle, revolving belt, or other mechanism designed to transfer the tested parts to the appropriate bins. These machines were designed to handle individual devices to match the typical capability of the testers of the day. For memory applications, testing soon evolved to four test sites. Packaging was still mainly Dual Inline Plastic (DIP).

A few years later, board technology started to migrate to surface mount, bringing up new package types. For the J-

lead and gull wing style of inline packaging, gravity handler technology evolved to fill the handling needs.

Also at this time, quad and array packaging started to become popular. Gravity handlers attempted to deal with this new technology by using carriers or nests to protect the device leads during handling, or by using "decelerators" to reduce device impact when the leads contacted the stops.

The decelerator approach was reasonably successful, but really only for robust quad packages like the Plastic Leaded Chip Carrier (PLCC) and Ceramic Leadless Chip Carrier (CLCC). While enabling safe handling, this technique reduced throughput. For packages where carriers were used, the carrier was often molded into the package during assembly and then removed after testing – adding extra material, or at least an extra process step. The use of molded carrier was probably the first major cooperation between package assembly and test handling. The use of carriers -- although adding to the cost of assembly – allowed some existing handling technology cope with evolving needs.

By the middle of the 1980s, it was becoming apparent to most test and manufacturing organizations that a new paradigm for handling was required. In response to that need, the first commercially successful pick-and-place handlers were built in the mid 1980s. The commercial success of these early systems brought about a number of robotic gantry pick-and-place handlers, as well as carrier/nest-based and turret-based pick-and-place handlers.

Interestingly, these pick-and-place and gravity handlers use completely different technology and each present a different outward appearance, even to a casual observer. Pick-and-place handlers usually have much less throughput than their gravity based counterparts, and are typically more expensive.

As these equipment evolutions took place, testing also continued to evolve – with more parallelism becoming the norm. As a result, most of today's gravity handlers have variants that support four test sites for short test time products, and pick-and-place handlers have further specialized to handle either short test times with up to eight units in parallel or long test times using 16 to 64 test sites.

The ultimate result of test handler evolution is that handlers are now mostly application specific – not only for package type, but also for test application – and as testing continues to evolve, even more diversification and specialization will likely occur.

For instance, gravity and pick-and-place handlers for short test time applications now have high speed sorting sections, some as fast as 28,000 units per hour for gravity handlers. Unfortunately, most real world applications limit the sorter throughput due to long test times and a limited number of test sites.

Further, they need to take devices out of transport media such as tubes or trays one at a time and assemble them in an array of 4 to 64 devices and present them to a test system. Ironically, most of these packages were already in multi-device arrays during the assembly process but have been cut up or "singulated" for test.

RESISTANCE TO PROCESS CHANGE

In many cases, conversion from traditional test handling (singulated packages) to a matrix approach requires an organizational change as well as a process change:

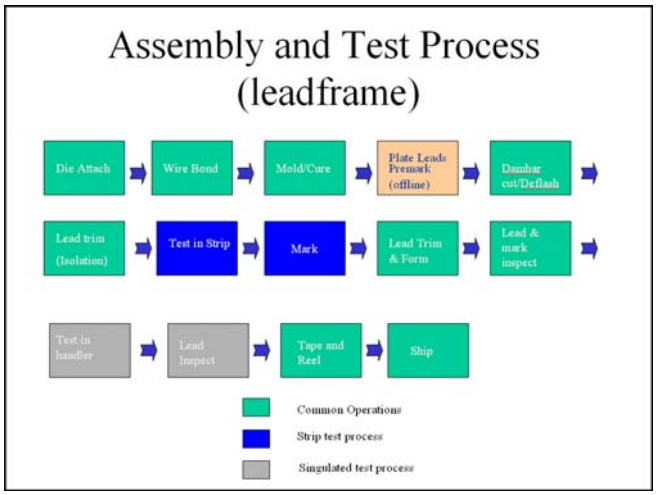

Figure 3

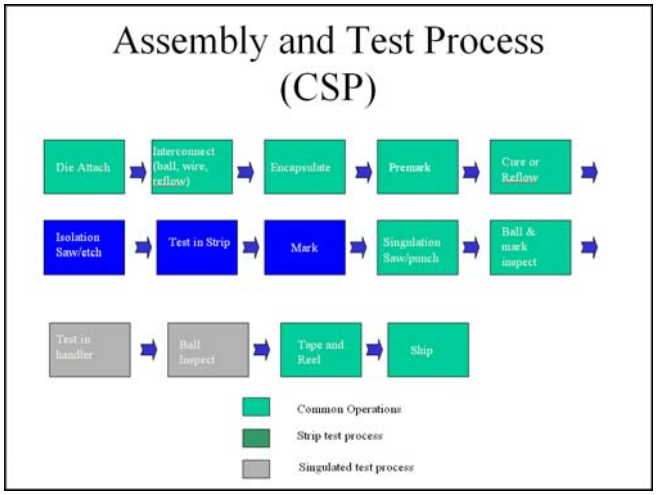

Figure 4

The degree of difficulty in implementing strip test is often related to the interdependence and ownership of the corporate resources that have responsibility for each major activity during the overall production process. In many cases, some or even all of these functional blocks are contracted out to different providers or are part of a different corporate group.

In some cases, organizational behavior gives the impression that dis-economies exist where they don't, and the overall

economic benefit of strip test is hidden. In these instances, the successful adoption of strip test requires significant organizational change.

For this reason, many companies perform strip test by proxy, using a subcontractor who has already developed the process. In fact, many of those farthest along in strip implementation are subcontract test and assembly providers. This makes sense as these companies profit directly by increasing the efficiencies of assembly and test.

However, it is important for organizations to realize they could receive the same efficiency gains from developing and implementing strip test processes on their own.

ASSEMBLY METHODS

All devices are in strip or matrix format at some point during their assembly process, but testing devices in this strip format adds some additional construction parameters that were not considered in the past. One of those is device isolation.

During traditional assembly, many devices are "bussed" or shorted together until they are "singulated" and placed in tubes or trays for final test. In some cases, the leadframe itself serves to hold the devices together during transport. In other cases devices in a panel or a substrate built on a PC board or film have typically one mask process to place the interconnect metal and leads, leaving all leads of all devices bussed together.

There are ways to overcome this problem for many package types, such as an isolation cut made by sawing, selective punch operation, laser or water jet. In general, many substrate package types are being designed to support strip testing from the start, with the individual devices being electrically isolated by adding in an extra mask/etch step during assembly.

Metal leadframe devices can be isolated prior to test by adding a trim operation, which can typically be done on existing trim form gear. Small devices with few leads can even be sourced and shipped untested from assembly subcontractors in this format.

Here are two examples of devices – one substrate and one leadframe – that were originally shorted, but have been isolated by sawing and reworked to be suitable for strip testing:

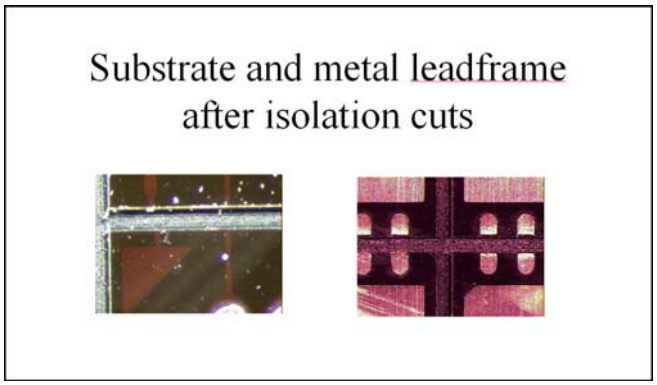

Figure 5

These devices could be processed in strip format by performing an isolation cut with a saw. In this method the strip is cut only to a depth that severs the device leads, leaving the overmold intact on the topside. This process is known as "de-bussing". It's also possible to cut only the device leads with a laser or etch process. Panel warpage often makes de-bussing of metal leadframe parts very difficult. In the next example, the panel warpage would require an isocut to follow the profile of the panel using a motorized prober Z stage to be successful:

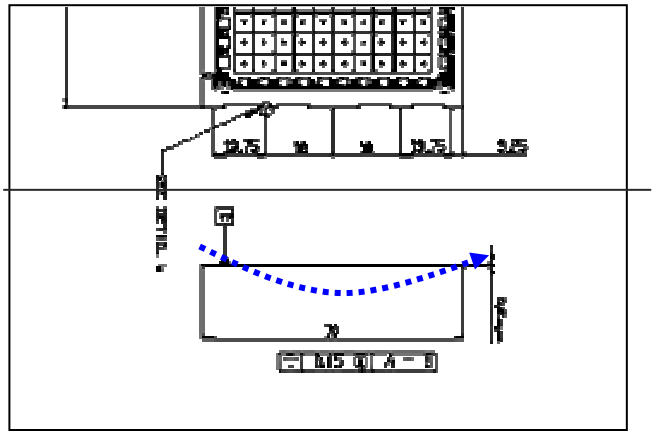

Figure 6

Other issues with de-bussing are as follows:

- Saw setup
  - Must compensate for blade wear
  - Must calculate depth and start/stop to keep strip intact, yet isolated
  - Strip may "shed" some leadframe parts during handling if isolation isn't done correctly
  - New leadframe design may be required in some cases
  - Appears to be possible
- Leadframe issues
  - Need to have minimum warpage
  - May need to redesign leadframe to avoid "shedding" metal parts
  - Some panels are too warped to isocut effectively; having warpage greater than

about 5mm across the width of the strip (about 35mm) with some individual devices warped about 1mm.

Overall, it would be far better to have isolated strips by design.

A final consideration for assembly is robustness after isolation. Some SOP leadframe designs lack structural integrity after lead trim, and also have very little area to accommodate high speed handling and alignment after isolation punch. It would be interesting to compare the costs involved with new leadframe design allowing for handling areas – basically a non consumed part of the metal leadframe – with the savings for test costs.

Another assembly method consideration for strip testing is strip density. In the past, device density on an assembly strip was determined by material usage and limitations of existing standard equipment. As devices sizes get smaller, however, more and more devices can be present in a typical strip.

This high device density is easily accommodated by strip testing, and some companies are beginning to make strips in high density specifically to take advantage of the increased throughput and parallel test capability these new formats offer.

Figure 7

Other high-density packages are Micro Lead Frame (MLF), Quad Flat No-lead (QFN) and micro Ball Grid Array (µBGA), all capable of having 96 to more than 200 devices in a strip depending on specific package size. On the fine pitch side, these packages have contact sizes down to about 150 microns and below. These dimensions are approaching those of wafer level test structures. According to the 2003 ITRS Roadmap for Assembly, BGA, CSP and FBGA bump sizes are currently as small as 160 microns, and will approach 100 microns in the next 10 years.

EXISTING TEST CAPABILITY – TESTERS AND CONTACTORS

Generally, older test systems with a limited number of pins and long test times can limit the benefits of strip test. Numerous top tier semiconductor testing operations still using these systems are "making do" in this industry downturn with antiquated test systems where the best case is about 3000 units per hour on a single or few test sites regardless of the handling method used.

Upgrading this tester technology – or adoption of DFT or BIST testing techniques -- is often the first step in strip test conversion. One notable exception, though, is in the linear and discrete area. Test times for these devices or components can be well under 100 milliseconds, making the throughput increase for strip test is significant even in single-site testing.

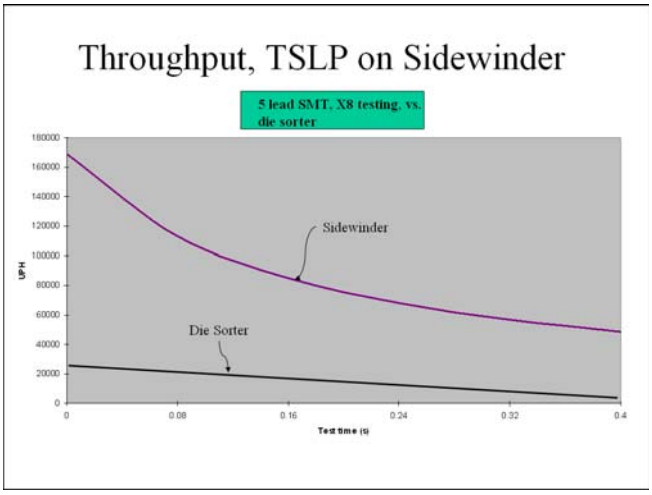

Figure 8

Fortunately, tester, load board and most importantly contactor and probe card technology have evolved to the point that – for many applications – high parallel test is indeed possible in very dense test arrays such as a high density strip format.

New testers and test techniques are available today that challenge long held standards of costs per pin, making higher parallel testing very attractive. In fact, since strip test allows greater parallel testing and minimizes device-handling overhead, high speed and high parallel testers are the most effective for strip test.

Contactors for strip test are available from many sources, and contactor construction for strip testing can be easier in some ways than that of singulated handling.

Traditionally, the contactors in traditional handlers are part of the mechanical design of the handler's test site mechanism. As test methodology has moved to contactors built primarily for their electrical properties, specialist companies – not handler companies – now make most of the

contactors in use on the test floor. These companies must work with and incorporate mechanical alignment features into their designs such that they are compatible with installed handlers.

Strip test handlers, on the other hand, typically have some kind of machine vision that determines precise contactor alignment using fiducial marks placed on the contactor body:

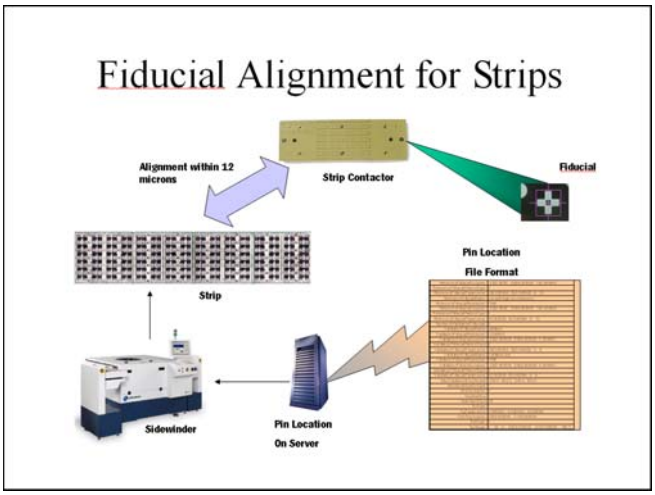

Figure 9

Another method that can be used to determine contactor alignment is "automatic probe-to-pad alignment" (APTPA), where the strip handler finds the contactor or probe pins automatically using the vision system. This technique allows the use of existing probe card technology to contact the smallest of device geometries:

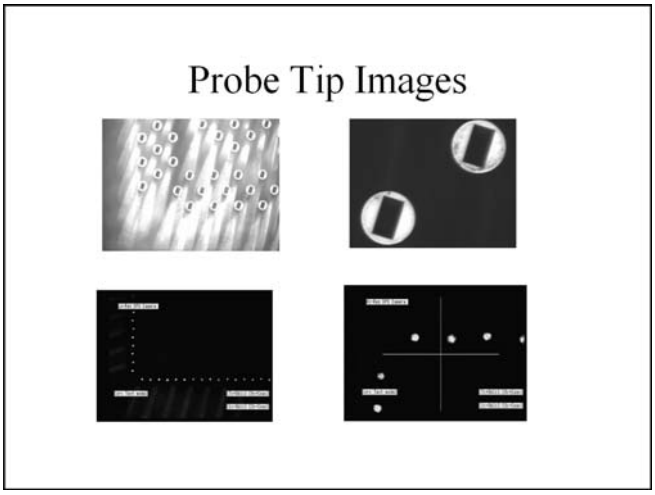

Figure 10

Through the use of these techniques, virtually any contactor or probe card technology can be adapted for strip testing. This freedom may allow for new technologies that produce better yields than those of established methods. Of course, device test correlation needs to be done carefully. Strip testing typically exhibits higher yields than traditional handlers due to the contactor flexibility as well as the very high precision of lead placement on the contact pins. Electroglas offers a web-based process management solution that can (among many other things) use tester bin data to monitor contact resistance and then automatically take action to resolve the problem.

TECHNOLOGY - STRIP TEST HANDLER

Strip handlers are by nature less mechanically complicated than their pick-and-place counterparts. Some would also argue that they are even less complicated than a quad site gravity handler. Although uncomplicated to operate, strip handlers have a lot of technology underneath the surface.

TECHNOLOGY – STRIP MAPPING SOFTWARE

Since the testing and sorting functions are performed on different machines during strip test, a positive means of identifying and tracking devices is required. This means that each strip carries a specific identification mark, and some manufacturers have gone to the level of specifically identifying each individual device within a strip.

In some strip testing lines for metal leadframes, like 0.150" Small Outline Integrated Circuit (SOIC), laser or ink marking is performed immediately after testing so that failed devices can be identified in existing trim and form equipment by either the lack of a mark, by a large "X" over the device top side, or by placing an ink dot over a pre-marked device. In this way strip test can be largely accommodated using existing assembly and marking/packing equipment, but with only one "good" bin possible. Rejects can be reclaimed by removing the ink mark and retesting in a conventional singulated handler. This implementation is often the lowest cost method of implementing strip test.

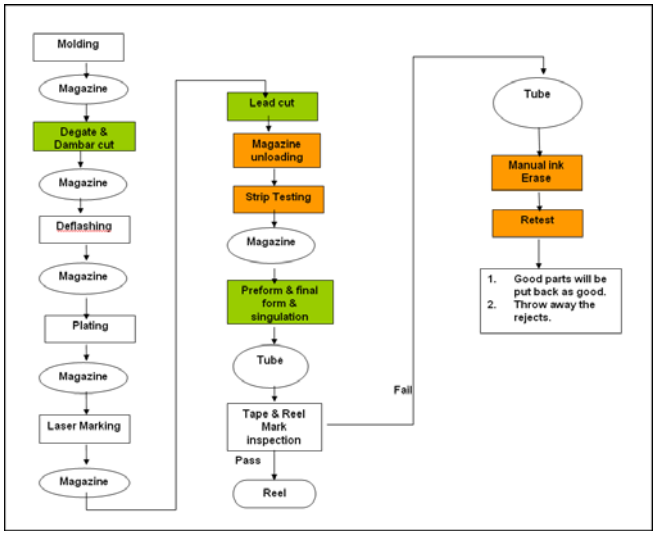

Figure 11

There is a SEMI standard for map data format, G85, at http://downloads.semi.org.

This format can be applied to wafers or strips, however, since strips are not all born as geometrically the same as wafers, it is useful to include more information about the strip layout with the map. This need is being addressed by a new SEMI standard proposal #3754 which describes how a detailed substrate layout may be expressed in XML.

There are many other potential benefits found in converting to a map-based, networked process – such as:

- Monitor and control production lines from any location – worldwide
- Collect, analyze and report critical test process information
- Perform OEE analysis and make reports automatically
- Direct corrective action needed — automatically

TECHNOLOGY – FUTURE TRENDS IN STRIP TEST

Future trends in strip test include:

- **Decreasing device size resulting in higher strip density.** Additionally, new device geometries will require machine vision to acceptably contact very small chip to board interconnect structures.

- **Larger strips with very dense device geometry.** This trend parallels the move to 300mm wafers. Larger matrices of devices reduce assembly and test costs.

- **Low cost implementation using existing assembly and test floor equipment.** The current downturn has driven manufacturers to enter the strip test area piecemeal, adding only the minimum equipment to get started in production and then work to optimize the process over time. Interestingly, the ASP of a typical strip handler is not much different than a traditional handler, while unit output in many test applications can be 10 to 20 times higher.

- **Higher parallel testing.** Tester manufacturers must "plant weeds in their own gardens" or risk losing out to competitors. New tester architecture allows more parallel testing at lower costs per pin.

- **Final test combined with Design for Test (DFT) and Built-in Self Test.** Complex and physically large devices with very long test times are not optimal for strip test, due to the relative amount of time spent on tester versus handling overhead. Final test in combination with DFT techniques can make some of these devices perform well for strip testing.

- **Increasing use of contract assembly and test.** Device manufacturers will rely on companies who can invest in and fully utilize new manufacturing technology while they concentrate on the business of designing the devices.

- **Decreasing costs for equipment.** Typical of the semiconductor industry, there is pricing pressure on strip handlers. If sold based on value (throughput), strip handlers should cost many millions of dollars. The overall pricing is influenced by "what's the going rate for a handler".

- **Individual device mapping and web based process management.** Web based process management is becoming the norm for advanced wafer sort floors, and will also propagate to strip testing as this process matures.

SUMMARY

With economics and technology both in favor of strip testing, it is somewhat surprising that the remaining hurdles – those being resistance to process change and the existence of older technologies that minimize the benefits of strip testing – have not come down more quickly.

As we have pointed out, however, several major manufacturers have already successfully adopted strip testing, and the advantages will soon be impossible to ignore for those who haven't. One way to ensure that happens is by sharing the results of early adopters, many of whom have published articles detailing the results of this process. Here are some links to these sources:

1. http://www.chipscalereview.com/issues/0300/assembly20.html
2. National Semiconductor article on strip implementation
3. http://www.future-fab.com/documents.asp?grID=217&d_ID=1681
4. ASM Matrix process
5. http://www.future-fab.com/documents.asp?d_ID=943
6. Motorola article on strip test implementation
7. http://www.analog.com/UploadedFiles/Technical_Quality_Papers_/34279446507178261735608033618656520672166891 46eos_esd_02_paper.pdf
8. Analog Devices article on strip testing ESD measurement
9. http://www.onboard-technology.com/online/200110/2601.html
10. Motorola singulation proposal for substrate packaging
11. http://dom.semi.org/web/wmagazine.nsf/0/5949232562cf541b882568ea00762792?OpenDocument
12. Jack Kessler article on strip implementation